Γεώργιος Κορνάρος

1. Γενικά Στοιχεία

Φορέας Απασχόλησης

Αναπληρωτής Καθηγητής
Τμήμα Ηλεκτρολόγων και Μηχανικών Υπολογιστών
Ελληνικό Μεσογειακό Πανεπιστήμιο Κρήτης
Εσταυρωμένος 71004, Ηράκλειο, Κρήτη
Τηλ.: +30 2810 379868, +30 2810 379168
Φαξ: +30 2810 371994

kornaros@hmu.gr

Ακροκορίνθου 9
71409, Ηράκλειο
Κρήτη, Ελλάδα
Τηλ: +30 6976085743

kornaros@gmail.com

1.1. Ερευνητικά Ενδιαφέροντα

Σχεδίαση και μεθοδολογίες για semi-/full-custom ψηφιακά κυκλώματα, Αρχιτεκτονικές πολλαπλών πυρήνων (multi- many-core), Cyber-physical Systems, Ενεργειακά αποδοτικές αρχιτεκτονικές, Ενσωματωμένα συστήματα, Ετερογενή και πολυ-πύρηνα συστήματα, Συστήματα αναδιατασσόμενης λογικής, Αρχιτεκτονικές συστημάτων επικοινωνίας υψηλών επιδόσεων.

1.2. Σύνοψη Ερευνητικού Έργου

Αρχικά εργάστηκε σε σχεδίαση του front- and back-end design of Telegraphos-II switch chip χρησιμοποιώντας semi-custom και full-custom VLSI σχεδίαση. Αργότερα συνείσφερε στον χαρακτηρισμό και υλοποίηση ψηφιακών συστημάτων με μνήμες multi-ported RAM and CAM για τον μεταγωγέα ATLAS single-chip switch για το ICS-FORTH. Στην εταιρία ISD SA ως τεχνικός διευθυντής του Digital Integrated Systems Group δούλεψε σε ερευνητικό έργο σε σχέση με αρχιτεκτονικές επεξεργαστών δικτύου σε συνεργασία με την εταιρία ST Microelectronics. Στην εταιρία Ellemedia Technologies Ltd σε συνεργασία με την εταιρία Lucent εργάστηκε σε τρία έργα (εθνικά και της ΕΕ) ως Τεχνικός Διευθυντής και επικεφαλής αρχιτέκτονας στην σχεδίαση επεξεργαστών δικτύων υψηλών ταχυτήτων σε ένα μοναδικό chip.

Στο ΤΕΙ Κρήτης παράλληλα με το διδακτικό και διοικητικό έργο ως Επίκουρος καθηγητής και Head του θεσμοθετημένου εργαστηρίου Ευφυών Συστημάτων (Intelligent Systems and Computer Architecture Lab), οι ερευνητικές δραστηριότητες επικεντρώνονται στην σχεδίαση αποδοτικών αρχιτεκτονικών ετερογενών πολυπύρηνων και ενσωματωμένων συστημάτων. Ειδικά, οι πρώτες ερευνητικές δραστηριότητες αφορούν την ανάπτυξη συσκευής Point-of-Care (integrated micro system for nucleic acid extraction, purification, PCR amplification, reagent mixing, biochemical reactions and finally DNA micro array detection in real time) για το έργο EU-funded project Micro2DNA και για την ανάπτυξη ενός Lab-on-Chip σε εθνικό έργο (EPAN-II). Οι πρόσφατες ερευνητικές δραστηριότητες συνοψίζονται σε αρχιτεκτονικές multi-core και ετερογενή συστημάτων και ειδικά στην σχεδίαση ειδικών ψηφιακών υποσυστημάτων υλικού για την βελτιστοποίηση ενσωματωμένων συσκευών με εικονικοποίηση (virtualization), καθώς και για την βελτιστοποίηση της μικροαρχιτεκτονικής ετερογενών επεξεργαστών/συστημάτων με στόχο την προσαρμοστικότητα, ασφάλεια και απόδοση (έργα EU projects VIRTICAL, SAVE, TRESCCA, DREAMS). Πιο πρόσφατα, στο έργο «TAPPS, Trusted Apps for open CPS, EU Horizon 2020» στόχος είναι να αναπτύξει ένα παράλληλο περιβάλλον Trusted Execution Environment (T.E.E.) πραγματικού χρόνου μέσω νέων μηχανισμών ασφαλείας που βασίζονται σε hardware, processor και network-centric τεχνικές, για άκρως αξιόπιστες εφαρμογές CPS στους τομείς εφαρμογών για την υγεία και την αυτοκινητοβιομηχανία.

1.3. Σπουδές

- University of Crete, Department of Computer Engineering and Electronics, Chania, Greece.
  Ph.D (2013)
  Thesis: "Real-time ASIC Monitoring for System-level Power and Thermal Management"

- University of Crete, Department of Computer Science, Heraklion, Greece.
  M.Sc. in Computer Science (Jun/1997). GPA 8.5/10.0
  Areas: Computer Architecture, VLSI design, High-Speed Networks and Communication Architectures.
  Thesis: "Implementation of Pipelined Multi-Queue Management in the ATLAS I Switch in Full-Custom CMOS VLSI"

- University of Patras, Department of Computer Engineering & Informatics, Patra, Greece.
  Diploma in Computer Engineering and Informatics (Jun/1992). GPA 8.53/10.00

2. Ακαδημαϊκή – Ερευνητική Εμπειρία

2.1. Διδακτικό/Διοικητικό Έργο

Ο Γ. Κορνάρος υπηρετεί στο Ελληνικό Μεσογειακό Πανεπιστήμιο, Σχολή Μηχανικών, έχοντας αναλάβει κατά καιρούς την οργάνωση και διδασκαλία των παρακάτω προπτυχιακών και μεταπτυχιακών μαθημάτων στο Τμήμα Ηλεκτρολόγων και Μηχανικών Υπολογιστών.

1999, 2001-2003, 3/2006 – τώρα Αναπληρωτής Καθηγητής – Τμήμα Ηλεκτρολόγων και Μηχανικών Υπολογιστών (Electrical and Computer Engineering Department) (formerly Informatics Engineering Department, and even formerly Applied Informatics and Multimedia Department – Technological Educational Institute of Crete (TEI)), **(**3/2006 – 5/2015 Lecturer**), στο Ελληνικό Μεσογειακό Πανεπιστήμιο (Hellenic Mediterranean University (HMU))**

- Teaching Undergraduate Courses:
  - Computer Architecture,
  - Digital Design,
  - System Digital Design with FPGAs
  - Microcontrollers/Microprocessors
  - Embedded Systems
- Teaching Graduate Courses:
  - Multi-core Architectures,
  - Advanced Embedded System Design

Ο Γ.Κορνάρος έχει επιβλέψει έναν αριθμό πτυχιακών εργασιών (20 προπτυχιακές και 4 μεταπτυχιακές) σχετικών με τα ερευνητικά του ενδιαφέροντα, ενώ αρκετές πτυχιακές εργασίες έχουν οδηγήσει σε δημοσιεύσεις σε διεθνή συνέδρια.

Ο Γ.Κορνάρος έχει συμμετάσχει σε έναν αριθμό επιτροπών για την διεκπεραίωση διοικητικών θεμάτων, όπως λόγου χάρη (α) Πρόεδρος της επιτροπής πρόχειρων διαγωνισμών του ΤΕΙ Κ. για το 2012-2013, β) Συντονισμός/οργάνωση κατεύθυνσης Μηχανικών Υπολογιστών στο νέο πρόγραμμα σπουδών, γ) Επιτροπή διοίκησης και διαχείρισης του κλειστού Γυμναστηρίου ΤΕΙ Κρήτης 2016-2017, δ) Προϊστάμενος Τομέα Πληροφορικής Τμήματος, μέλος Συμβουλίου Τμήματος 2017 κ.α.

2.2. Ερευνητικά Προγράμματα (Ευρωπαϊκά και Ελληνικά)

15/10/2019 – 14/10/2022 EL.ME.PA Scientific Coordinator – EU/H2020 Project acronym: **AVANGARD**, Project full title: "Advanced manufacturing solutions tightly aligned with business needs", Grant agreement no: 869986

The AVANGARD project addresses the integration of three novel processing units into an existing Microfactory test bed conceived to produce urban electric vehicles. The units are state of-the-art multipurpose and multifunctional demonstrators on their own, specifically:

- Robotized integration of laser cutting-shaping-welding for 3D components
- Supersonic deposition of metallic powders for high speed 3D printing
- Large volume and high-speed 3D polymeric printing

The operation of the AVANGARD pilot will be demonstrated manufacturing I-Bikes, I-CARS and innovative battery packs. (http://www.avangard-project.eu)

1/01/2015 – 31/12/2017 TEI Crete Scientific Coordinator – EU/H2020 Project acronym: **TAPPS**, Project full title: "Trusted Apps for Open CPS", Grant agreement no: 645119, H2020-ICT-01-2014 Smart Cyber-Physical Systems (EU Funding 3,885,484 €, TEI: 255.462,50€) (H2020-ICT/RIA/TAPPS 645119)

TAPPS is a Research and Innovation Action (RIA) European project which provides and validates an end-to-end solution for development and deployment of trusted apps, including an App Store and a model-based tool chain for trusted application development. The role of TEI is to extend the execution environment inside the System Control Units and exploit functionalities provided by the novel hardware-, processor- and network-centric security mechanisms for on-chip and off-chip communications. http://www.tapps-project.eu/ (1/01/2015 – 31/12/2017).

1/09/2013 – 1/09/2016 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **SAVE**, Project full title: "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures", Grant agreement no: 610996, FP7-ICT-2013-10 (EU Funding 2,930,000 €, TEI: 424.000,00 €) (FP7-ICT/STREP/SAVE 610996)

SAVE is a European collaborative research project funded within the Seventh Framework Programme (FP7) aimed at the development of software/hardware technologies for an efficient exploitation of *heterogeneous system architectures*. In the SAVE project HW/SW/OS components are developed that allow for deciding at runtime the mapping of the computation kernels on the appropriate type of resource, based on the current system context and requirements. http://www.fp7-save.eu/ (1/9/2013 – 31/08/2016)

1/10/2012 – 1/10/2015 Member – EU/FP7 Project acronym: **TRESCCA**, Project full title: "TRustworthy Embedded systems for Secure Cloud Computing Applications", Grant agreement no: 318036 Collaborative project FP7-ICT-2011-8 (EU contribution: 2,950,000 €, TEI: 428.158,00 €)

The TRESCCA project aims to lay the foundations of a secure and trustable cloud platform by ensuring strong logical and physical security on the edge devices, using both hardware security and virtualization techniques while considering the whole cloud architecture. http://www.trescca.eu/index.php. (01/10/2012-30/09/2015)

1/10/2013 – 1/10/2017 Member – EU/FP7 Project acronym: **DREAMS,** Project full title: "Distributed REal-time Architecture for Mixed Criticality Systems" (FP7-ICT IP DREAMS 610640, TEI: 745.600,00 €)

The objective of DREAMS is to develop a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality, executing on networked multi-core chips, are supported. DREAMS will deliver architectural concepts, meta-models, virtualization technologies, model-driven development methods, tools, adaptation strategies and validation, verification and certification methods for the seamless integration of mixed-criticality to establish security, safety, real-time performance as well as data, energy and system integrity.

DREAMS is one of three projects funded by the European Commission in the area of mixed-criticality systems from the FP7 ICT call 10. The EC financial contribution amounts to 11 million euros.
http://www.dreams-project.eu/

15/07/2011 – 15/07/2014 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **VIRTICAL**, Project full title: "SW/HW extensions for virtualized heterogeneous multicore platforms ", Grant agreement no: 288574 Theme [ICT-2011.3.4: Computing Systems] (EU Contribution: 2,860,000 €, TEI: 378.880,00 €)

The vIrtical project aims to increase functionality, reliability and security of embedded devices at sustainable cost and power consumption. This is achieved in the vIritical project by extending the virtualization concept of the general-purpose domain to the embedded domain. In order to expand the virtualization concept to the embedded devices, this project will deliver software/hardware extensions at different layers of the design stack (hardware, operating system, hypervisor and applications) to increase flexibility, programmability, performance, QoS, reliability, security and power saving. http://www.virtical.eu/

1/06/2012 – 1/06/2015 Member of Main Research Team – "Application Specific Hierarchical Shared Memory (ASHSHMEM)", Υποέργο 31 με τίτλο «Ιεραρχικά Κοινόχρηστα Συστήματα Μνήμης για Ενσωματωμένες Εφαρμογές» στο πλαίσιο της πράξης "ΑΡΧΙΜΗΔΗΣ ΙΙΙ - ΕΝΙΣΧΥΣΗ ΕΡΕΥΝΗΤΙΚΩΝ ΟΜΑΔΩΝ ΣΤΟ ΤΕΙ ΚΡΗΤΗΣ" Χρηματοδοτικός φορέας: ΕΠΕΔΒΜ- Επιχειρησιακό Πρόγραμμα "Εκπαίδευση και Δια Βίου Μάθηση" (Συνολικός προϋπολογισμός: 82 k€)

10/2009 – 09/2010 TEI Crete Scientific Coordinator – "Στοιχεία Μικροηλεκτρονικής για Lab-On-Chip Όργανα Μοριακών Αναλύσεων για Γενετικές και Περιβαλλοντικές Εφαρμογές"- Lab-On-Chip-ATEI-CRETE, Corallia Microelectronics Cluster, ΜΙΚΡΟ2-39/Ε-ΙΙ-Γ, Φάση-2 Ενίσχυσης Ελληνικών Τεχνολογικών Συνεργατικών Σχηματισμών στη Μικροηλεκτρονική/ΜΙΚΡΟ2-ΣΕ-Γ/Ε-ΙΙ, Ε.Π. Ανταγωνιστικότητα και Επιχειρηματικότητα (ΕΠΑΝ-ΙΙ) – Π.Ε.Π. Περιφερειών Μεταβατικότητας Στήριξης (συνολικού προϋπολογισμού 3,084,885 €), 1/10/2009-31/12/2012

6/2006 – 6/2009 Center for Research & Technology TEI Crete – **EU/FP6** Project acronym: **Micro2DNA**

Worked under the FP6-IST-4-027333-STP project Micro^{2}DNA "Integrated polymer-based micro-fluidic micro-system for DNA extraction, amplification, and silicon-based detection", designing the electronic part of the embedded system for the Point-of-Care device.

3. Επαγγελματική Εμπειρία

5/2001 – 12/2005 Employed by *Ellemedia Technologies*, Athens.
Founder and Technical Manager of the Ellemedia Technologies Crete Dept.

- Working on WEBSoC (GSRT Project), a network processor on a VirtexII-Pro FPGA responsible for Queue Management and Scheduling components, and chip integration. - EUREKA E!3326 WEBSoC (Wireless Ethernet Bridging System-on-Chip)
- Working on NP-MADE on hardware scheduler and traffic shaper components. - EUREKA E!3132 NP-MADE (Network Processor for Multi-service Access Devices)
- Previously worked on *PRO3* (the Protocol Processor Project, IST 11499), a single chip network processor (fabricated with a standard 0.18um cmos technology by UMC), as hardware designer of the Scheduler sub-blocks. Architectural design, implementation, and synthesis of Scheduling Components and memory interfaces.

2/2000 – 4/2001 Employed by *Integrated Systems Development (**ISD**)*, Athens
Technical Manager of the Digital Integrated Systems Group, **Founder** of ISD-Crete Dept.

- **ISD** collaborates with France based **SGS Thomson Microelectronics** (ST Microelectronics) developing IPs for Telecom applications, memories for Low-Power devices and methodology for embedded system verification. Managed the development of BroadBand Network Terminal (BBNT), specifying the architecture and verification methodology in collaboration with the AST – ST group. BBNT is a system on chip, combining 8 physical ATM links of aggregate bandwidth 155 Mbps, 8 Ethernet 10/100 links, and supporting multiple protocols (ATM, AAL0, AAL5, Ethernet switching, VLAN and DIX support, IP over ATM, MPOA, LANE v1 and v2) with the aid of embedded CPU cores.

- Consulting services to CARV group (Computer Architecture & VLSI) of the Computer Science Institute, Foundation of Research and Technology, Heraklio (FORTH), regarding network architectures and VLSI design.

1/1999 – 6/2000 Employed by *Institute of Computer Science, Foundation of Research & Technology* (***ICS – FORTH***), Heraklion

- Member of Computer Architecture and VLSI systems group (CARV). Worked on ATLAS-II, an optimized version of ATLAS, a 16x16 single chip ATM switch. In Front-End (FE) using Synopsys tools, Verilog and Verisure, optimized sub-blocks of ATLAS. In Back-End (BE) compacted ATLAS to nearly 50% using full-custom design techniques whenever beneficial. Used Unicad Design Kit under Cadence DFWII, Silicon Ensemble.

3/1998 – 12/1998

- Worked under the ASICCOM project, integrating ATLAS and performing the placement and routing of the chip, as well as the verification (DRC, ERC, LVS). Used extensively Preview Cell3 Ensemble, CELL3, Silicon Ensemble, Cadence DIVA/DRACULA verification products, Unicad Tools (by SGS-Thomson). ATLAS I is a 16x16 single chip ATM switch that provides advanced flow control (multilane back-pressure), a large on-chip cell buffer (256 cells), aggregate bandwidth of 10Gb/s and supports three priority levels, multiple logical queues and efficient multicasting. ATLAS I was designed in a 0.35micron CMOS process using 6 million transistors, and was taped-out for fabrication on November 1998.

6/1996 – 3/1998

- Designed the queue management subsystem of ATLAS switch, implementing three-ported and four-ported SRAMs, CAM blocks Priority Enforcer and peripheral circuits in full-custom VLSI.
- Characterized the full-custom blocks of ATLAS and developed verilog models (**8/97 – 3/98)**.
  Used Analog Artist, Virtuoso Layout Editor, Spice, Hspice, Anacad Tools (ELDO, Xelga), Verilog.

6/1994 – 5/1995

- As a member of the CARV group designed and implemented Telegraphos II Switch (Semi-Custom Design with ES2 CMOS ecpd07 0.7um process), a single switch chip with four-by-four unidirectional point-to-point links, providing 1.2 Gbps aggregate throughput with DDR techniques, and featuring shared buffering, virtual circuit (VC) level, credit-based flow control, and cut-through.
- Used Verilog, ES2 design kit under the Cadence DFW. Telegraphos is a project to design architectures and build prototypes for high speed computer communication, in Networks of Workstations or Workstation Clusters.

4. Ακαδημαϊκές Δραστηριότητες

4.1. Διοργανώσεις – Παρουσιάσεις

[1] European Forum for Electronic Components and Systems (EFECS), H2020 EU-TAPPS Demonstration/Presentation, 5-7 Dec 2017, **DOI:** 10.13140/RG.2.2.21366.45126

[2] DATE 2017 Tutorial "The Internet of INSECURE Things", Organizer: Marcello Coppola, STMicroelectronics, FR, George Kornaros, TEI Crete, GR, Giovanni Gherardi, Energica Motor Company, IT, Presentation: G. Kornaros, "Using a Secure IoT Platform Based on STM32 MCUs"

[3] IEEE/ACM Design, Automation and Test in Europe (DATE) 2013, Embedded Tutorial: "From Embedded Multi-core SoCs to Scale-out Processors", Marcello Coppola, Babak Falsafi, John Goodacre, George Kornaros, March 20, 2013

[4] HiPEAC 2014, January 20-22, 2014 | Vienna Austria Workshop/Tutorial VVITEMES, "First Workshop on Vertical Virtualization Techniques in Heterogeneous Multicore Embedded Systems", María Engracia Gómez, Andrea Marongiu, Sergey Tverdyshev, Marcello Coppola, Georges Kornaros, Davide Bertozzi and José Flich

[5] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010, Conference Co-Chairman – Organizer (M. Grammatikakis – G. Kornaros)

4.2. Κριτής σε Περιοδικά – Συνέδρια, Μέλος Επιτροπών Συνεδρίων

[1] Reviewer, Computers Journal, www.mdpi.com/journal/computers, Oct 2018
[2] Reviewer, Journal: Microprocessors and Microsystems, May 2018
[3] Reviewer, Computers-OpenAccess Journal, http://www.mdpi.com/journal/computers, Apr 2018
[4] Reviewer, ACM Journal on Emerging Technologies in Computing Systems, Mar 2018
[5] Reviewer, Journal: Microprocessors and Microsystems, Dec 2017 Elsevier B.V.
[6] Reviewer: IEEE Transactions on VLSI (Oct'17)
[7] Reviewer: IEEE Transactions on Multi-Scale Computing Systems (2017)
[8] Reviewer: Journal JLPEA (ISSN 2079-9268), http://www.mdpi.com/journal/jlpea/special_issues/embedded_systems
[9] Program Committee in Mobile Networks for Biometric Data Analysis (mBiDa 2014)
[10] Reviewer, ACM TODAES, 2014
[11] Reviewer, IEEE Transaction on Parallel and Distributed Systems (IEEE TPDPS), 2013
[12] Reviewer, IEEE Transaction on Computers (IEEE TC), 2012
[13] Reviewer, Elsevier JSA, 2012
[14] Reviewer, ACM TRETS, 2013
[15] Reviewer, CRC Press (www.crcpress.com), Series: Embedded Multi-Core Systems
[16] Participation in IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 26 July - 6 August, 2010, Aveiro, Portugal
[17] IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 18 July - 1 August, 2009, Kiel, Germany

[18] Reviewer, IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2011, Regensburg, July 7-8, 2011, 2012, 2013

[19] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010

Conference Co-Chairman – Organizer

[20] Reviewer, ASIC/SOC Conference 2011

[21] Reviewer, Design, Automation and Test in Europe Conference (DATE'2010)

[22] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2009 Ancona, Italy, June 25-26, 2009

Session Chairman

[23] DSD'2003 EUROMICRO Symposium on Digital System Design, Architectures, Methods and Tools, Antalya, Turkey, September 3 – 5, 2003, Session Chairman

4.3. Πατέντες

[1] "**Apparatus for use in a CAN system**"
Publication number US2018 / 0295112 A1
Publication date Oct 11, 2018
Application number US 15/939,598
Filing date Mar. 29, 2018
Inventors: Antonio - Marcello Coppola , Sassenage (FR) ; Georgios Kornaros , Crete (GR) ; Giovanni Gherardi , Pelago (IT)

[2] Title: "APPARATUS FOR USE IN A CAN SYSTEM"
Greek Application No. 20170100160, filed on April 5, 2017
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Giovanni Gerardi
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete, Energica S.p.A.

[3] "**Apparatus and methods implementing dispatch mechanisms for offloading executable functions**"
Publication number US20170206169 A1
Publication type Application
Application number US 15/402,515
Publication date Jul 20, 2017
Filing date Jan 10, 2017
Priority date Jan 15, 2016
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US20170206169

[4] "**Resource access control in a system-on-chip**"
Publication number US9519596 B2
Publication type Grant
Application number US 14/629,613
Publication date Dec 13, 2016
Filing date Feb 24, 2015
Priority date Mar 6, 2014
Also published as US20150254189
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US9519596

[5] Inventor(s): Antonio-Marcello COPPOLA. George Kornaros. Miltos Grammatitakis.
Title: **"System Address-Space Protection/Security Service Support at the Network-on-Chip"**
Application for patent has been filed on 06 Mar 2014, Invention Ref: 13-GR2CO-0333.

4.4. Δημοσιεύσεις

4.4.1. Δημοσιεύσεις σε Περιοδικά

Journals

[1] O. Tomoutzoglou, D. Mbakoyiannis, G. Kornaros and M. Coppola, "Efficient Job Offloading in Heterogeneous Systems through Hardware-assisted Packet-based Dispatching and User-level Runtime Infrastructure," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
doi: 10.1109/TCAD.2019.2907912
URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8675484&isnumber=6917053

[2] George Kornaros, Othon Tomoutzoglou and Marcello Coppola, "Hardware-assisted Security in Electronic Control Units Utilizing One-Time-Programmable Network-on-Chip and Firewalls", IEEE Micro, Volume: 38, Issue: 5, Sep./Oct. 2018, pp. 63-74, 2018
DOI: https://ieeexplore.ieee.org/abstract/document/8474944

[3] Dimitrios Mbakoyiannis, Othon Tomoutzoglou, and George Kornaros. 2018. **Energy-Performance Considerations for Data Offloading to FPGA-Based Accelerators Over PCIe**. ACM Transactions on Architecture and Code Optimization, 15, 1, Article 14 (March 2018), 24 pages. DOI: https://doi.org/10.1145/3180263

[4] Ioannis Christoforakis, Maria Astrinaki, and George Kornaros. 2018. **Towards architectural support for bandwidth management in mixed-critical embedded systems**. SIGBED Review 14, 4 (January 2018), 21-26. DOI: https://doi.org/10.1145/3177803.3177807

[5] Miltos D. Grammatikakis, Kyprianos Papadimitriou, Polydoros Petrakis, Antonis Papagrigoriou, George Kornaros, Ioannis Christoforakis, Othon Tomoutzoglou, George Tsamis, Marcello Coppola, "**Security in MPSoCs: A NoC Firewall and an Evaluation Framework**", IEEE Trans. on CAD of Integrated Circuits and Systems, vol 34 – 8, pp.1344-1357, 2015, DOI: 10.1109/TCAD.2015.2448684

[6] G. Kornaros and D. Pnevmatikatos, "**Dynamic Power and Thermal Management of NoC-based Heterogeneous MPSoCs**", *ACM Transactions on Reconfigurable Technology and Systems* (TRETS), Volume 7 Issue 1, February 2014
Article No. 1, 26 pages. DOI=10.1145/2567658 http://doi.acm.org/10.1145/2567658

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